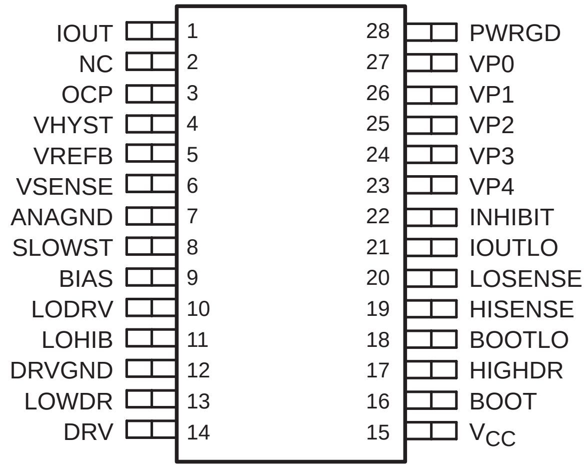
- **Single-Channel, 5-V Controller**
- **Synchronous-Rectifier Drivers for Greater Than 90% Efficiency**
- **Useable for All Common DSP Supply Voltages – Popular Output Voltage Options Set With Program Pins**
- **EVM Available**
- **Ideal for Applications With Current Ranges From 3 A to 30 A.**
- **Hysteretic Control Technique Enables Fast Transient Response — Ideal for ’C6000 or Multiple ’C5000 Applications**
- **Low Supply Current**
  - **− 3 mA in Operation**
  - **− 90 µA in Standby**
- **Power Good Output**
- **28-Pin TSSOP PowerPAD™ Package**

PWP PACKAGE
(TOP VIEW)

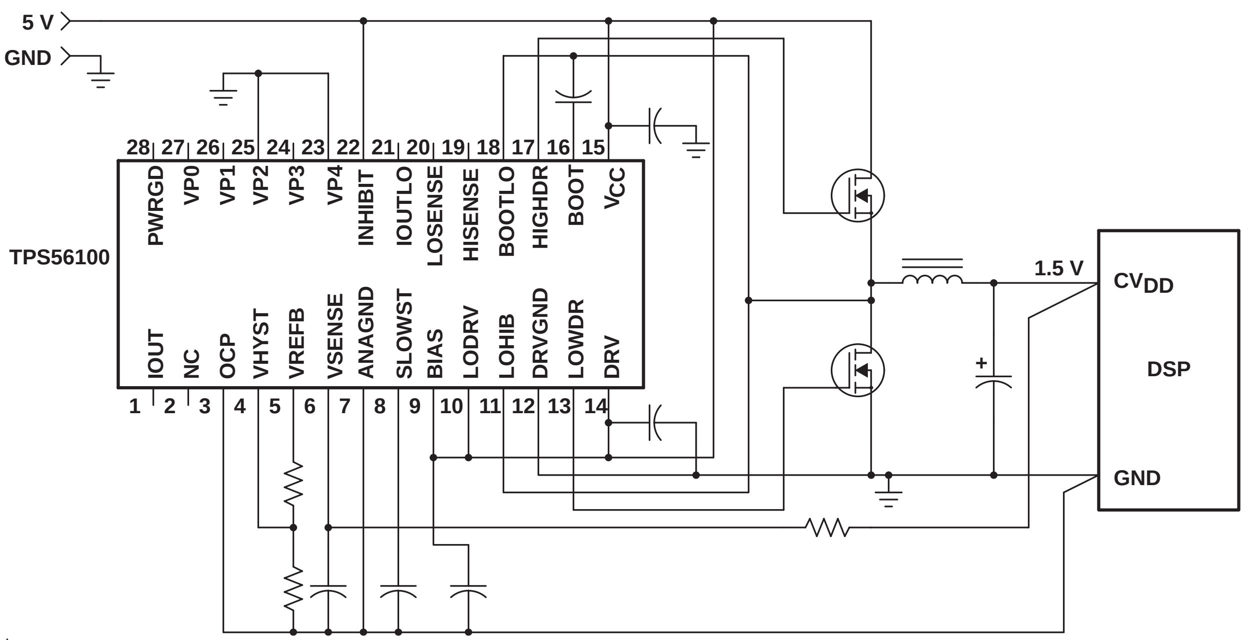


NC − Not Connected

description

The TPS56100 is a high-efficiency synchronous-buck regulator controller which provides an accurate programmable supply voltage to low-voltage digital signal processors, such as the ‘C6x and ‘C54x DSPs. An internal 5-bit DAC is used to program the reference voltage from 1.3 V to 2.6 V. Higher output voltages can be implemented using an external input resistive divider. The TPS56100 uses a fast hysteretic control method that provides a quick transient response. The propagation delay from the comparator input to the output driver is

application example



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description (continued)

less than 300 ns, even at maximum output current. Overcurrent shutdown and crossover protection combine to eliminate destructive faults in the output MOSFETs, thereby protecting the processor during operation. The slowstart current source is proportional to the reference voltage, thereby eliminating variation of the slowstart timing when changes are made to the output voltage. When the output drops to less than 93% of the nominal output voltage, PWRGD will pull the open-drain output low. The overvoltage circuit will disable the output drivers if the output voltage rises more than 15% above the nominal output voltage. The TPS56100 also includes an inhibit input to control power sequencing and undervoltage lockout thereby insuring the 5-V supply is within limits before the controller starts. The 2-A MOSFET drivers can power multiple MOSFETs in parallel to drive single or multiple DSPs and load currents up to 30 A. The high-side driver can be configured as a ground-referenced driver or as a floating bootstrap driver with the included internal bootstrap Schottky diode.

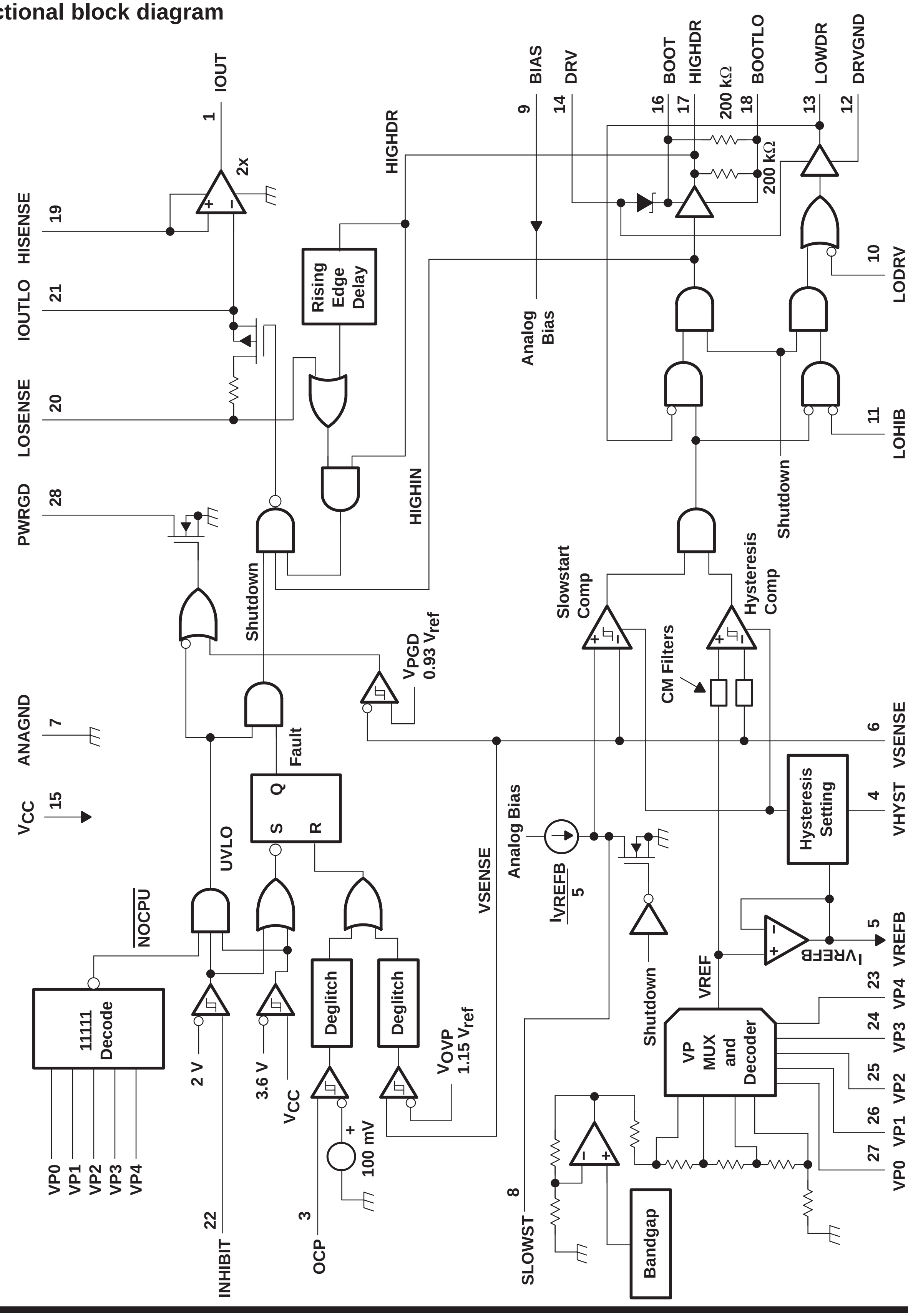
The TPS56100 is available in a 28-pin TSSOP PowerPAD package, which increases thermal efficiency and eliminates bulky heat sinks.

AVAILABLE OPTIONS

T_J	PACKAGES	EVM
	TSSOP† (PWP)	
0°C to 125°C	TPS561000PWP	TPS56100EVM−128

† The PWP package is also available taped and reel. To order, add an R to the end of the part number (e.g., TPS561000PWPR).

functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ANAGND	7	I	Analog ground
BIAS	9	I	Analog BIAS pin. This terminal must be connected to 5-V supply voltage. A 1-µF ceramic capacitor should be connected from BIAS to ANAGND.
BOOT	16	I	Bootstrap. Connect a 1-µF low-ESR capacitor from BOOT to BOOTLO.
BOOTLO	18	I	Bootstrap low. Connect BOOTLO to the junction of the high-side and low-side FETs for floating drive configuration. Connect BOOTLO to PGND for ground reference drive configuration.
DRV	14	I	Drive bias for the FET drivers. This terminal must be connected to 5-V supply voltage. A 1-µF ceramic capacitor should be connected from DRV to DRVGND.
DRVGND	12	I	Drive ground. Ground for FET drivers. Connect to FET PWRGND.
HIGHDR	17	O	High drive. Output drive to high-side power switching FETs
HISENSE	19	I	High current sense. For current sensing across high-side FETs, connect to the drain of the high-side FETs; for optional resistor sensing scheme, connect to power supply side of current-sense resistor placed in series with high-side FET drain.
INHIBIT	22	I	Disables the drive signals to the MOSFET drivers.
IOUT	1	O	Current out. Output voltage on this pin is proportional to the load current as measured across the Rds(on) of the high-side FETs. The voltage on this pin equals $2 \times R_{ds(on)} \times IOUT$. In applications where very accurate current sensing is required, a sense resistor should be connected between the input supply and the drain of the high-side FETs.
IOUTLO	21	O	Current sense low output. This is the voltage on the LOSENSE pin when the high-side FETs are on. A ceramic capacitor should be connected from IOUTLO to HISENSE to hold the sensed voltage while the high-side FETs are off. Capacitance range should be between 0.033 µF and 0.1 µF.
LODRV	10	I	Low drive enable. Normally tied to 5 V. To activate the low-side FETs as a crowbar, pull LODRV low.
LOHIB	11	I	Low side inhibit. Connect to the junction of the high and low side FETs to control the anti-cross-conduction and eliminate shoot-through current. Disabled when configured in crowbar mode.
LOSENSE	20	I	Low current sense. For current sensing across high-side FETs, connect to the source of the high-side FETs; for optional resistor sensing scheme, connect to high-side FET drain side of current-sense resistor placed in series with high-side FET drain.
LOWDR	13	O	Low drive. Output drive to synchronous rectifier FETs
NC	2		Not connected
OCP	3	I	Over current protection. Current limit trip point is set with a resistor divider between IOUT and ANAGND.
PWRGD	28	O	Power good. Power Good signal goes high when output voltage is within 7% of voltage set by VID pins. Open-drain output.
SLOWST	8	O	Slow Start (soft start). A capacitor from SLOWST to ANAGND sets the slowstart time. Slowstart current = $I_{VREFB}/5$
V_{CC}	15	I	5-V supply. A 1-µF ceramic capacitor should be connected from V_{CC} to DRVGND.
VHYST	4	I	HYSTERESIS set pin. The hysteresis is set with a resistor divider from V_{REFB} to ANAGND. The hysteresis window = $2 \times (V_{REFB} - V_{HYST})$
VP0	27	I	Voltage programming input 0
VP1	26	I	Voltage programming input 1
VP2	25	I	Voltage programming input 2
VP3	24	I	Voltage programming input 3
VP4	23	I	Voltage programming input 4. Digital inputs that set the output voltage of the converter. The code pattern for setting the output voltage is located in Table 1. Internally pulled up to 5 V.
VREFB	5	O	Buffered reference voltage from VP network
VSENSE	6	I	Voltage sense Input. To be connected to converter output voltage bus to sense and control output voltage. It is recommended that an RC low pass filter be connected at this pin to filter noise.

detailed description

V_{REF}

The reference/voltage programming (VP) section consists of a temperature-compensated bandgap reference and a 5-bit voltage selection network. The 5 VP terminals are inputs to the VP selection network and are TTL-compatible inputs internally pulled up to 5 V. The VP codes conform to the Intel *VRM 8.3 DC-DC Converter Specification* for voltage settings between 1.8 V and 2.6 V, and they are decremented by 50 mV, down to 1.3 V, for the lower VP settings. Voltages higher than V_{REF} can be implemented using an external resistive divider. Refer to Table 1 for the VP code settings. The output voltage of the VP network, V_{REF}, is within ±1.5% of the nominal setting over the VP range of 1.3 V to 2.6 V, including a junction temperature range of 0°C to +125°C. The output of the reference/VP network is indirectly brought out through a buffer to the V_{REFB} pin. The voltage on this pin will be within 2% of V_{REF}. It is not recommended to drive loads with V_{REFB}, other than setting the hysteresis of the hysteretic comparator, because the current drawn from V_{REFB} sets the charging current for the slowstart capacitor. Refer to the slowstart section for additional information.

hysteretic comparator

The hysteretic comparator regulates the output voltage of the synchronous-buck converter. The hysteresis is set by 2 external resistors and is centered about V_{REF}. The 2 external resistors form a resistor divider from V_{REFB} to ANAGND, with the output voltage connecting to the V_{HYST} pin. The hysteresis of the comparator will be equal to twice the voltage *difference* between the V_{REFB} and V_{HYST} pins. The propagation delay from the comparator inputs to the driver outputs is 300 ns (maximum). The maximum hysteresis setting is 60 mV.

low-side driver

The low-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The bias to the low-side driver is derived from DRV.

high-side driver

The high-side driver is designed to drive low-Rds(on) n-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured either as a ground-referenced driver or as a floating bootstrap driver. When configured as a floating driver, the bias voltage to the driver is developed from DRV. The internal bootstrap diode connected between the DRV and BOOT pins is a Schottky for improved drive efficiency. The maximum voltage that can be applied between BOOT and DRVGND is 30 V. The driver can be referenced to ground by connecting BOOTLO to DRVGND, and connecting BOOT to a voltage supply.

deadtime control

Deadtime control prevents shoot-through current from flowing through the main power FETs during switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate-drive voltage to the low-side FETs is below 2 V; the low-side driver is not allowed to turn on until the voltage at the junction of the high-side and low-side FETs (Vphase) is below 2 V.

current sensing

Current sensing is achieved by sampling and holding the voltage across the high-side power FETs while the high-side FETs are on. The sampling network consists of an internal 85-Ω switch and an external ceramic hold capacitor. Recommended value of the hold capacitor is between 0.033 µF and 0.1 µF. Internal logic controls the turnon and turnoff of the sample/hold switch such that the switch does not turn on until the Vphase voltage transitions high, and the switch turns off when the input to the high-side driver goes low. The sampling will occur only when the high-side FETs are conducting current. The voltage on the IOUT pin equals 2 times the sensed high-side voltage. In applications where a higher accuracy in current sensing is required, a sense resistor can be placed in series with the high-side FETs, and the voltage across the sense resistor can be sampled by the current sensing circuit.

detailed description (continued)

inhibit

INHIBIT is a TTL-compatible digital input used to enable the controller. When INHIBIT is low, the output drivers are low and the slowstart capacitor is discharged. When INHIBIT goes high, the short across the slowstart capacitor is released and normal converter operation begins. The 5-V supply must be above UVLO thresholds before the controller is allowed to start up. The inhibit start threshold is 2.1 V and the hysteresis is 100 mV for the INHIBIT comparator.

V_{CC} undervoltage lockout (UVLO)

The undervoltage lockout circuit disables the controller while the V_{CC} supply is below the 4-V start threshold during power up. When the controller is disabled, the output drivers will be low and the slowstart capacitor is discharged. When V_{CC} exceeds the start threshold, the short across the slowstart capacitor is released and normal converter operation begins. There is a 0.5-V hysteresis in the undervoltage lockout circuit for noise immunity.

slowstart

The slowstart circuit controls the rate at which V_O powers up. A capacitor is connected between SLOWST and ANAGND and is charged by an internal current source. The current source is proportional to the reference voltage, so that the charging rate of C_{SLOWST} is proportional to the reference voltage. By making the charging current proportional to V_{REF}, the power-up time for V_O will be independent of V_{REF}. Thus, C_{SLOWST} can remain the same value for all VP settings. The slowstart charging current is determined by the following equation:

$$I_{slowstart} = I(V_{REFB}) / 5 \quad \text{(amps)}$$

Where $I(V_{REFB})$ is the current flowing out of V_{REFB}.

It is recommended that no additional loads be connected to V_{REFB}, other than the resistor divider for setting the hysteresis voltage. The maximum current that can be sourced by the V_{REFB} circuit is 500 µA. The equation for setting the slowstart time is:

$$t_{SLOWST} = 5 \times C_{SLOWST} \times R_{VREFB} \qquad \text{(seconds)}$$

Where R_{VREFB} is the total external resistance from V_{REFB} to ANAGND.

power good

The power-good circuit monitors for an undervoltage condition on V_O. If V_O is 7% below V_{REF}, then the PWRGD pin is pulled low. PWRGD is an open-drain output.

overvoltage protection

The overvoltage protection (OVP) circuit monitors V_O for an overvoltage condition. If V_O is 15% above V_{REF}, then a fault latch is set and both output drivers are turned off. The latch will remain set until V_{CC} goes below the undervoltage lockout value or INHIBIT is low. A 3-µs deglitch timer is included for noise immunity. Refer to the LODRV section for information on how to protect the microprocessor against overvoltages due to a shorted high-side power FET.

detailed description (continued)

overcurrent protection

The overcurrent protection (OCP) circuit monitors the current through the high-side FET. The overcurrent threshold is adjustable with an external resistor divider between IOUT and ANAGND, with the divider voltage connected to the OCP pin. If the voltage on OCP exceeds 100 mV, then a fault latch is set and the output drivers are turned off. The latch will remain set until V_{CC} goes below the undervoltage lockout value and back up above 3.6 V or INHIBIT is similarly brought below its stop threshold and back above its start threshold. A 3-µs deglitch timer is included for noise immunity. The OCP circuit is also designed to protect the high-side power FET against a short-to-ground fault on the terminal common to both power FETs.

LODRV

The LODRV circuit is designed to protect the microprocessor against overvoltages that can occur if the high-side power FETs become shorted. External components sensing an overvoltage condition are required to use this feature. When an overvoltage fault occurs, the low-side FETs are used as a crowbar. LODRV is pulled low and the low-side FET will be turned on, overriding all control signals inside the TPS5210 controller. The crowbar action will short the input supply to ground through the faulted high-side FETs and the low-side FETs. A fuse in series with V_{in} should be added to disconnect the short circuit.

Table 1. Voltage Programming Codes

VP TERMINALS (0 = GND, 1 = floating or pull-up to 5 V)					V_{REF}
VP4	VP3	VP2	VP1	VP0	(Vdc)
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	No CPU
1	1	1	1	0	2.10
1	1	1	0	1	2.20
1	1	1	0	0	2.30
1	1	0	1	1	2.40
1	1	0	1	0	2.50
1	1	0	0	1	2.60

Table 1. Voltage Programming Codes (Continued)

VP TERMINALS (0 = GND, 1 = floating or pull-up to 5 V)					V_{REF}
VP4	**VP3**	**VP2**	**VP1**	**VP0**	**(Vdc)**
1	1	0	0	0	2.60
1	0	1	1	1	2.60
1	0	1	1	0	2.60
1	0	1	0	1	2.60
1	0	1	0	0	2.60
1	0	0	1	1	2.60
1	0	0	1	0	2.60
1	0	0	0	1	2.60
1	0	0	0	0	2.60

absolute maximum ratings over operating virtual junction temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note1), BIAS, DRV . . . . −0.3 V to 7 V
Input voltage range: BOOT to DRVGND (High-side Driver ON) . . . . −0.3 V to 30 V
BOOT to HIGHDRV . . . . −0.3 V to 15 V
BOOT to BOOTLO . . . . −0.3 V to 15 V
INHIBIT, VPx, LODRV . . . . −0.3 V to 7.3 V
PWRGD, OCP . . . . −0.3 V to 7 V
LOHIB, LOSENSE, IOUTLO, HISENSE . . . . −0.3 V to 7 V
VSENSE . . . . −0.3 V to 5 V
Voltage difference between ANAGND and DRVGND . . . . ±0.5 V
Output current, V_{REFB} . . . . 0.5 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . 0°C to 125°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to ANAGND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
PWP	1150 mW	11.5 mW/°C	630 mW	460 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	4.5	6	V
Input voltage, BOOT to DRVGND	0	28	V
Input voltage, BOOT to BOOTLO	0	13	V
Input voltage, INHIBIT, VPx, LODRV, PWRGD, OCP	0	6	V
Input voltage, LOHIB, LOSENSE, IOUTLO, HISENSE, BIAS, DRV	0	6	V
Input voltage, VSENSE	0	4.5	V
Voltage difference between ANAGND and DRVGND	0	±0.2	V
Output current, V_{REFB}†	0	0.4	mA

† Not recommended to load V_{REFB} other than to set hystersis since I_{VREFB} sets slowstart time.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 5 V (unless otherwise noted)

reference/voltage programming

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	Cumulative voltage reference accuracy	V_{CC} = 4.5 to 5.5 V, 1.3 V ≤ V_{REF} ≤ 2.6 V, See Note 2	−1.5%		1.5%	
VPx	High-level input voltage		2.25			V
VPx	Low-level input voltage				1	V
V_{REFB}	Output voltage	I_{VREFB} = 50 µA	V_{REF}−10 mV	V_{REF}	V_{REF}+10 mV	V
V_{REFB}	Output regulation	10 µA ≤ I_O ≤ 500 µA		2		mV
VPx	Input pullup resistance			190		kΩ

NOTES: 2. Cumulative reference accuracy is the combined accuracy of the reference voltage and the input offset voltage of the hysteretic comparator. Cumulative accuracy equals the average of the high-level and low-level thresholds of the hysteretic comparator.
3. This parameter is ensured by design and is not production tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 5 V (unless otherwise noted) (continued)

power good

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Undervoltage trip threshold		90	93	95	$\%V_{REF}$
V_{OL}	Low-level output voltage	I_O = 2.5 mA		0.4	0.75	V
I_{OH}	High-level input current	V_{PWRGD} = 5 V		1		µA
V_{hys}	Hysteresis voltage			3		$\%V_{REF}$

slowstart

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Charge current	V_{SLOWST} = 0.5 V, V_{VREFB} = 1.3 V, I_{VREFB} = 65 µA	10.4	13	15.6	µA
Discharge current	V_{SLOWST} = 1 V	3			mA
Comparator input offset voltage		−18		18	mV
Comparator input bias current	See Note 3		10	100	nA
Comparator hysteresis		−8.5		8.5	mV

NOTE 3: This parameter is ensured by design and is not production tested.

hysteretic comparator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage	See Note 3	−4		4	mV
Input bias current	See Note 3			500	nA
Hysteresis accuracy	$V_{REFB} - V_{HYST}$ = 15 mV (Hysteresis window = 30 mV)	−5		5	mV
Maximum hysteresis setting	$V_{REFB} - V_{HYST}$ = 30 mV		60		mV

NOTE 3: This parameter is ensured by design and is not production tested.

thermal shutdown

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Over temperature trip point	See Note 3		160		°C
Hysteresis	See Note 3		10		°C

NOTE 3: This parameter is ensured by design and is not production tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 5 V (unless otherwise noted) (continued)

high-side VDS sensing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Gain			2		V/V
	Initial accuracy	$V_{HISENSE}$ = 5 V, $V_{LOSENSE}$ = 4.5 V	194		206	mV
IOUTLO	Sink current	V_{IOUTLO} = 5 V			250	nA
IOUT	Source current	V_{IOUT} = 0.5 V, $V_{HISENSE}$ = 5 V, V_{IOUTLO} = 4.5 V	500			µA
IOUT	Sink current	V_{IOUT} = 0.05 V, $V_{HISENSE}$ = 5 V, V_{IOUTLO} = 5 V	50			µA
	Output voltage swing	$V_{HISENSE}$ = 4.5 V, R_{IOUT} = 10 kΩ	0		1	V
		$V_{HISENSE}$ = 3 V, R_{IOUT} = 10 kΩ	0		0.75	V
LOSENSE	High-level input voltage	$V_{HISENSE}$ = 4.5 V (see Note 3)	2.85			V
	Low-level input voltage				2.4	V
	Sample/hold resistance	4.5 V ≤ $V_{HISENSE}$ ≤ 5.5 V, LOSENSE connected to HISENSE, $V_{HISENSE} - V_{IOUTLO}$ = 0.15 V	62	85	123	Ω
		3 V ≤ $V_{HISENSE}$ ≤ 3.6 V, LOSENSE connected to HISENSE, $V_{HISENSE} - V_{IOUTLO}$ = 0.15 V	67	95	144	
CMRR		$V_{HISENSE}$ = 5.5 V to 3 V, $V_{HISENSE} - V_{OUTLO}$ = 100 mV	62	65		dB

NOTE 3. This parameter is ensured by design and is not production tested.

inhibit

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		1.85	2.1	2.35	V
Hysteresis		0.08	0.1	0.14	V
Stop threshold		1.76			V

overvoltage protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overvoltage trip threshold		112	115	120	$\%V_{REF}$
Hysteresis	See Note 3		10		mV

NOTE 3: This parameter is ensured by design and is not production tested.

overcurrent protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OCP trip threshold		80	100	125	mV
Input bias current				100	nA

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 5 V (unless otherwise noted) (continued)

deadtime

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOHIB	High-level input voltage		2.4			V
	Low-level input voltage				1.33	
LOWDR	High-level input voltage	See Note 3	2.38			V
	Low-level input voltage	See Note 3			1.23	

NOTE 3: This parameter is ensured by design and is not production tested.

LODRV

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LODRV	High-level input voltage		1.70			V
	Low-level input voltage				0.95	

input undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		3.8	4.08	4.46	V
Hysteresis		0.4	0.5	0.6	V
Stop threshold		3.3			V

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 5 V (unless otherwise noted) (continued)

output drivers

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output current (see Note 4)	High-side sink	Duty cycle < 2%, t_{pw} < 100 µs, T_J = 125°C, $V_{BOOT} - V_{BOOTLO}$ = 4.5 V,	0.7			A
	High-side source	V_{HIGHDR} = 0.5 V (source) or 4 V (sink), See Note 3	1.2			
	Low-side sink	Duty Cycle < 2%, t_{pw} < 100 µs, T_J = 125°C, V_{DRV} = 4.5 V,	1.3			
	Low-side source	V_{LOWDR} = 0.5 V (source) or 4 V (sink), See Note 3	1.4			
Output resistance (see Note 4)	High-side sink	T_J = 125°C, $V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 4 V (source) or 0.5 V (sink)			5	Ω
	High-side source				75	
	Low-side sink	T_J = 125°C, V_{DRV} = 4.5 V, V_{LOWDR} = 4 V (source) or 0.5 V (sink)			9	
	Low-side source				75	

NOTES: 3. This parameter is ensured by design and is not production tested.
4. The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{ds(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range		4.5	5	5.5	V
V_{CC}	Quiescent current	$V_{INHIBIT}$ = 5 V, VP code ≠ 11111, V_{CC} > 4.46 V at startup, V_{BOOTLO} = 0 V		3	10	mA
		$V_{INHIBIT}$ = 5 V, VP code ≠ 11111, V_{CC} > 4.46 V at startup, V_{BOOTLO} = 0 V, C_{HIGHDR} = 50 pF, C_{LOWDR} = 50 pF, f_{SWX} = 200 kHz, See Note 3		5		
	High-side driver quiescent current	$V_{INHIBIT}$ = 0 V or VP code = 11111 or V_{CC} < 3.8 V at startup, V_{BOOT} = 13 V, V_{BOOTLO} = 0 V			90	µA
		$V_{INHIBIT}$ = 5 V, VP code ≠ 11111, V_{CC} > 4.46 V at startup, V_{BOOT} = 13 V, V_{BOOTLO} = 0 V, C_{HIGHDR} = 50 pF, f_{SWX} = 200 kHz (see Note 3)		2		mA

NOTE 3: This parameter is ensured by design and is not production tested.

switching characteristics over recommended operating virtual-junction temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay	VSENSE to HIGHDR or LOWDR (excluding dead-time)	1.3 V ≤ V_{VREF} ≤ 2.6 V, 10 mV overdrive (see Note 3)		230	300	ns
	OCP comparator	See Note 3		1		µs
	OVP comparator			1		
	PWRGD comparator			1		
	SLOWST comparator	Overdrive = 10 mV (see Note 3)		700	1000	ns
Rise and fall time	HIGHDR output	C_L = 6 nF, V_{BOOT} = 4.5 V, V_{BOOTLO} = 0 V, T_J = 125°C			120	ns
	LOWDR output	C_L = 6 nF, V_{DRV} = 4.5 V, T_J = 125°C			80	
Deglitch time (Includes comparator propagation delay)	OCP	See Note 3	2		5	µs
	OVP		1.8		5	
Response time	High-side VDS sensing	$V_{HISENSE}$ = 4.5 V, V_{IOUTLO} pulsed from 4.5 V to 4.4 V, 100 ns rise/fall times (see Note 3)			3	µs
		$V_{HISENSE}$ = 3 V, V_{IOUTLO} pulsed from 3 V to 2.9 V, 100 ns rise/fall times (see Note 3)			3	
Short-circuit protection rising-edge delay	SCP	LOSENSE = 0 V (see Note 3)	300		500	ns
Turnon/turnoff delay	V_{DS} sensing sample/hold switch	3 V ≤ $V_{HISENSE}$ ≤ 5.5 V, $V_{LOSENSE}$ = $V_{HISENSE}$ (see Note 3)	30		100	ns
Crossover delay time	LOWDR to HIGHDRV, and LOHIB to LOWDR	See Note 3	50		200	ns
Prefilter pole frequency	Hysteretic comparator	See Note 3		5		MHz
Propagation delay	LODRV	See Note 3			400	ns

NOTE 3: This parameter is ensured by design and is not production tested.

TYPICAL CHARACTERISTICS

SLOWSTART TIME
vs
SLOWSTART CAPACITANCE

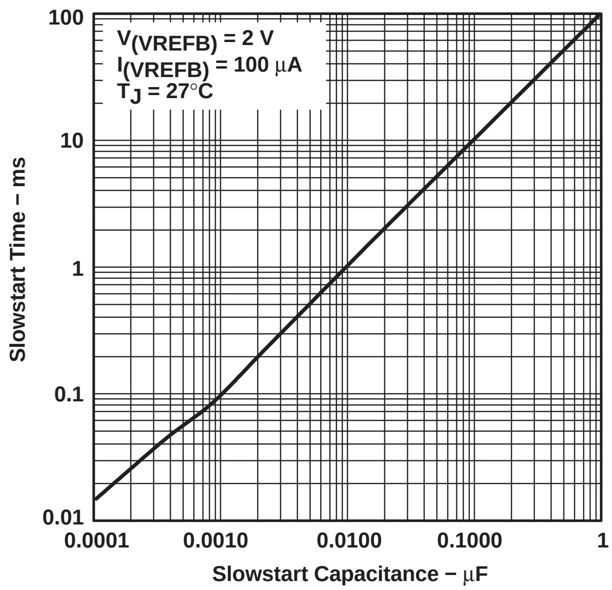


Figure 1

SLOWSTART TIME
vs
SUPPLY CURRENT (VREFB)

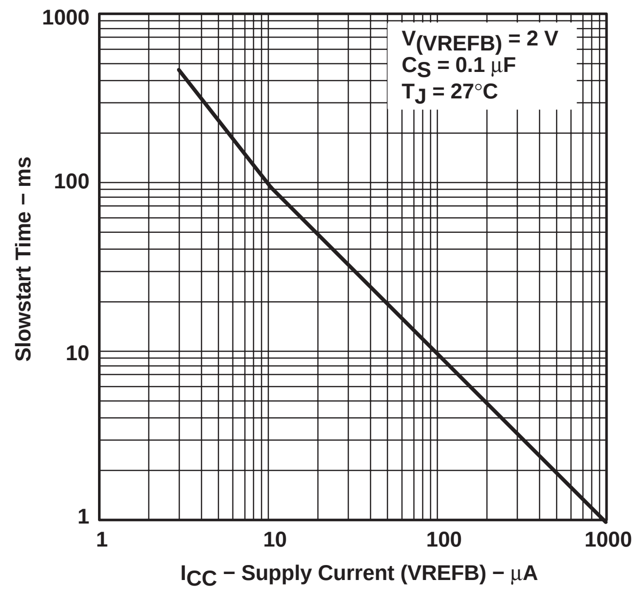


Figure 2

DRIVER
RISE TIME
vs
LOAD CAPACITANCE

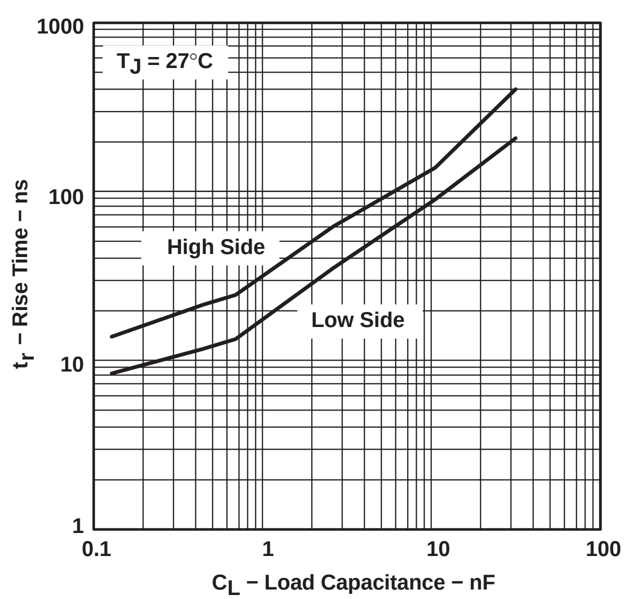


Figure 3

DRIVER
FALL TIME
vs
LOAD CAPACITANCE

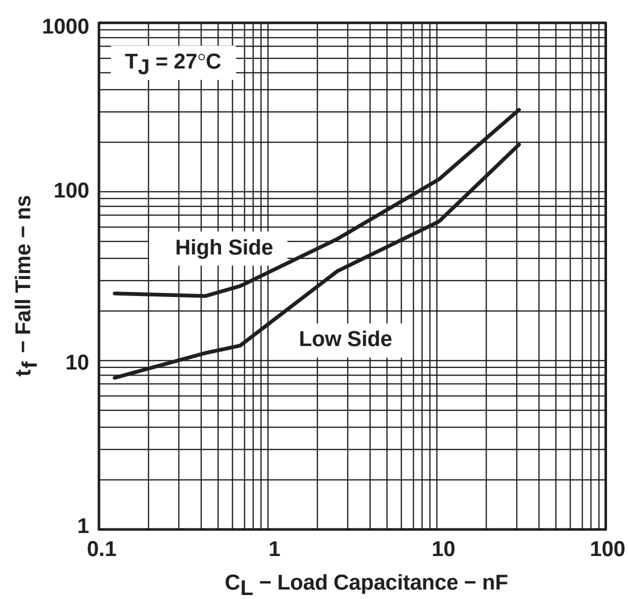


Figure 4

TYPICAL CHARACTERISTICS

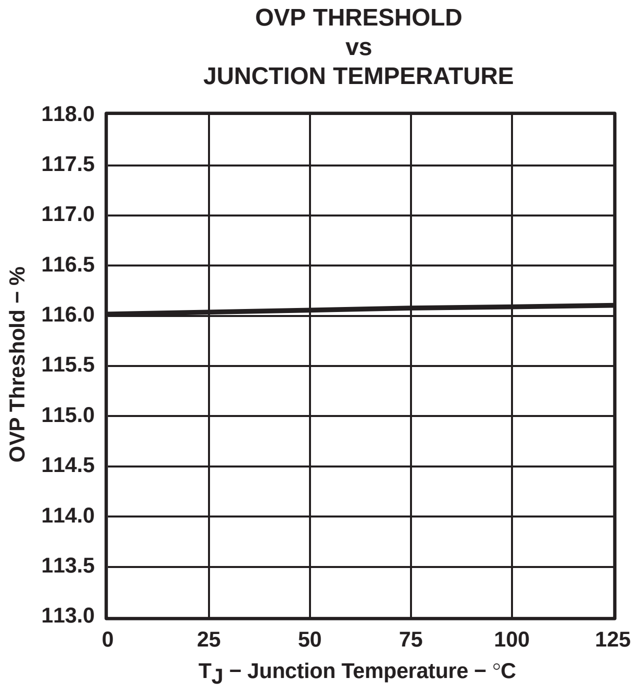


Figure 5

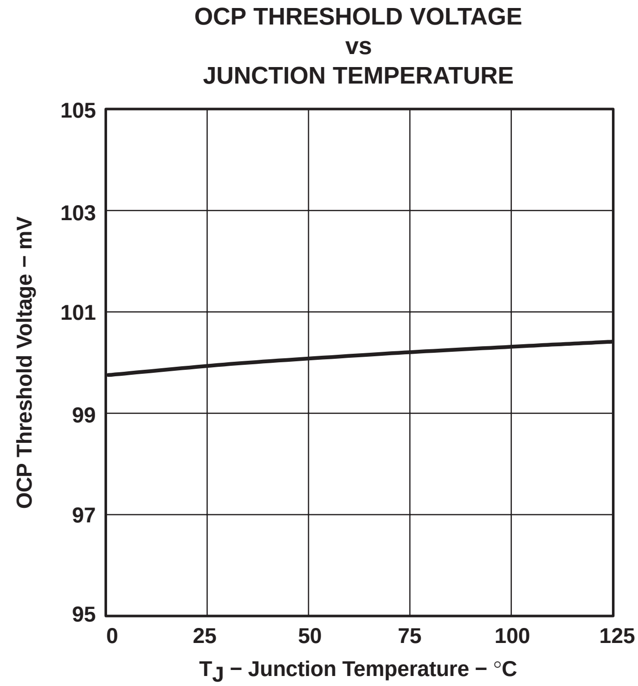


Figure 6

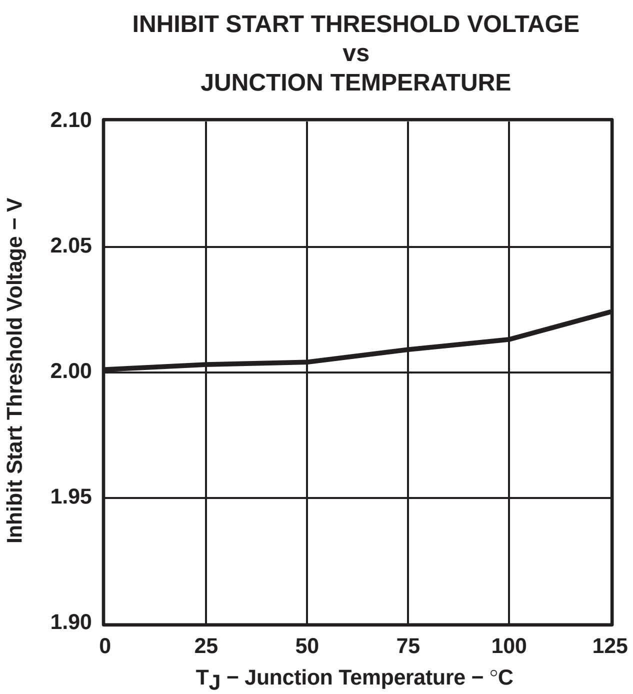


Figure 7

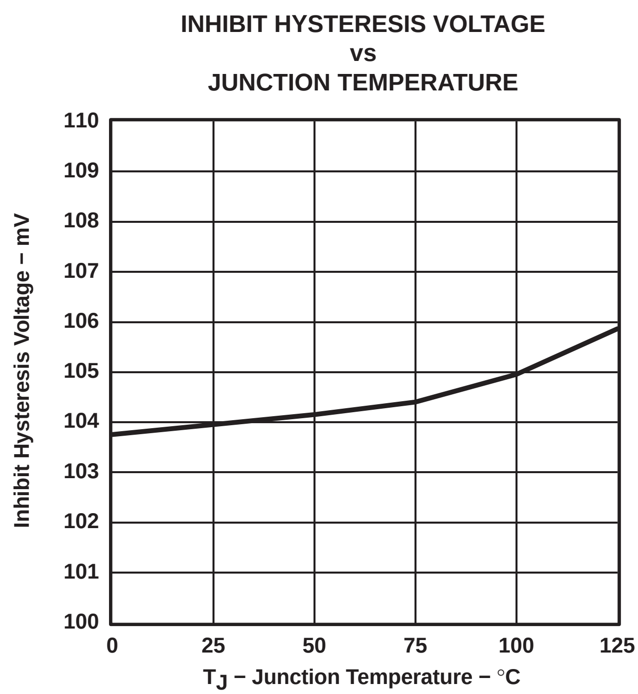


Figure 8

TYPICAL CHARACTERISTICS

UVLO START THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

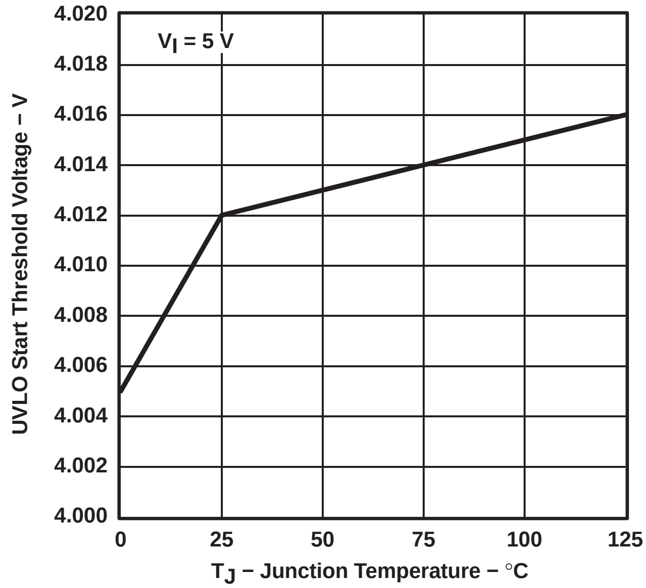


Figure 9

UVLO HYSTERESIS
vs
JUNCTION TEMPERATURE

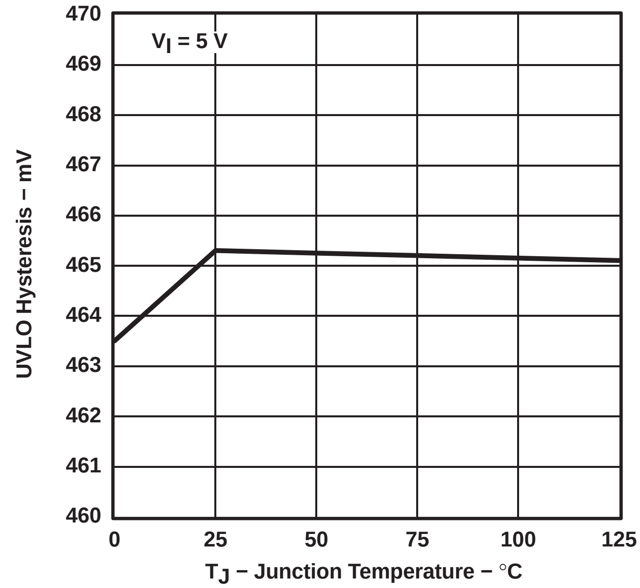


Figure 10

QUIESCENT CURRENT
vs
JUNCTION TEMPERATURE

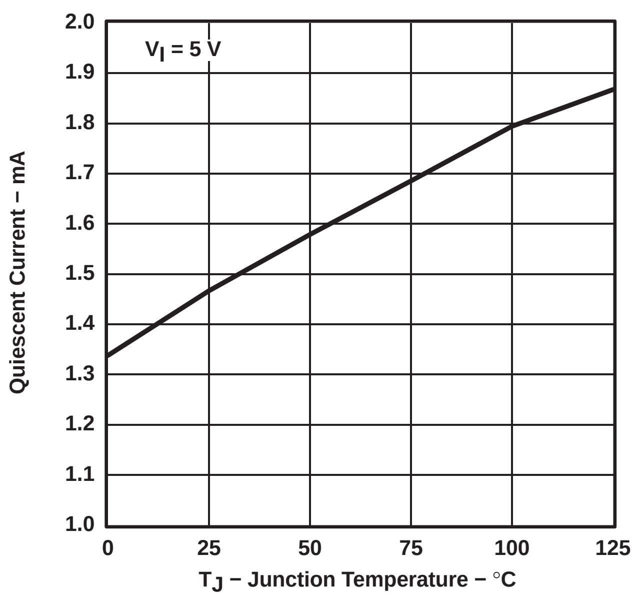


Figure 11

POWERGOOD THRESHOLD
vs
JUNCTION TEMPERATURE

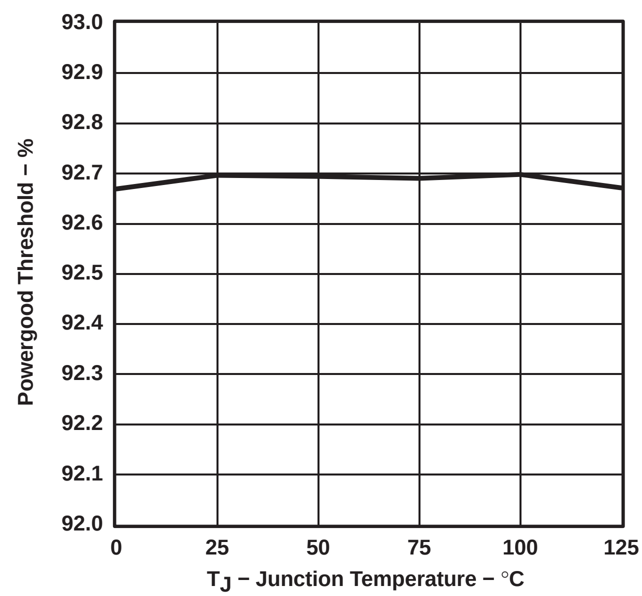


Figure 12

TYPICAL CHARACTERISTICS

SLOW START CHARGE CURRENT vs JUNCTION TEMPERATURE

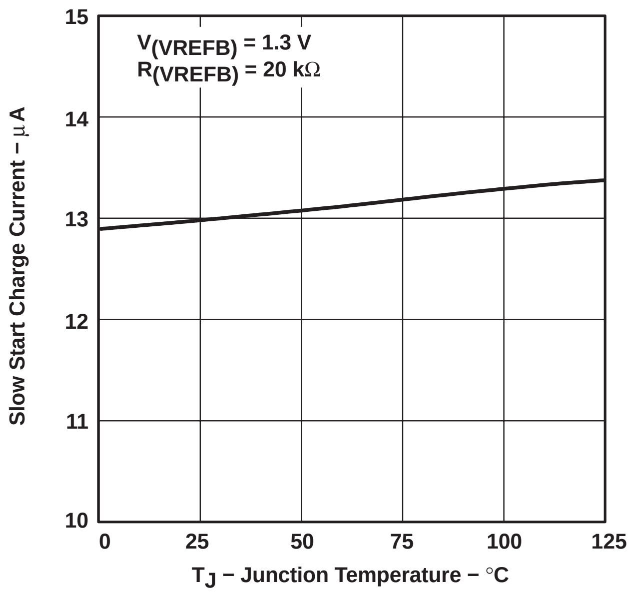


Figure 13

DRIVER HIGH-SIDE OUTPUT RESISTANCE vs JUNCTION TEMPERATURE

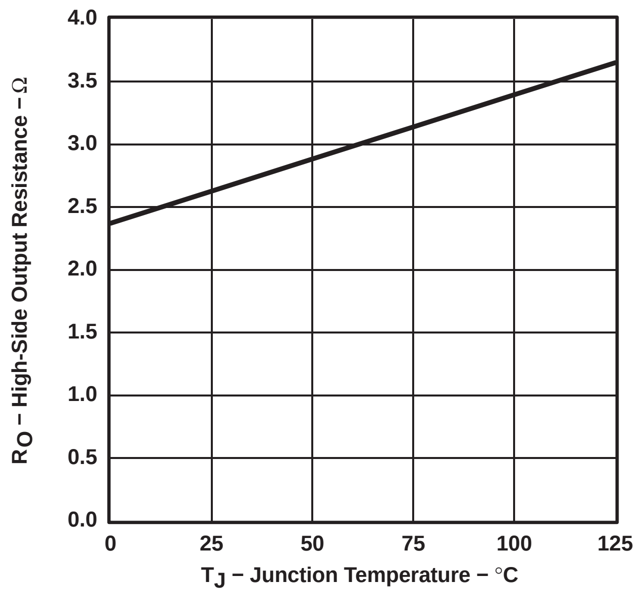


Figure 14

DRIVER LOW-SIDE OUTPUT RESISTANCE vs JUNCTION TEMPERATURE

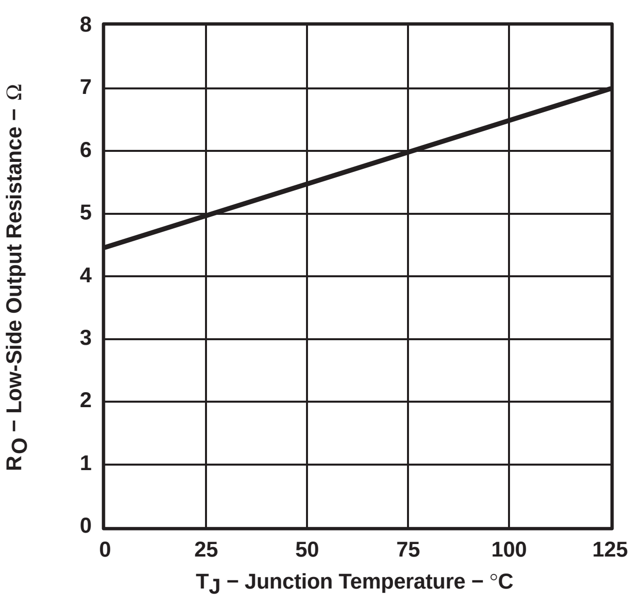


Figure 15

SENSING SAMPLE/HOLD RESISTANCE vs JUNCTION TEMPERATURE

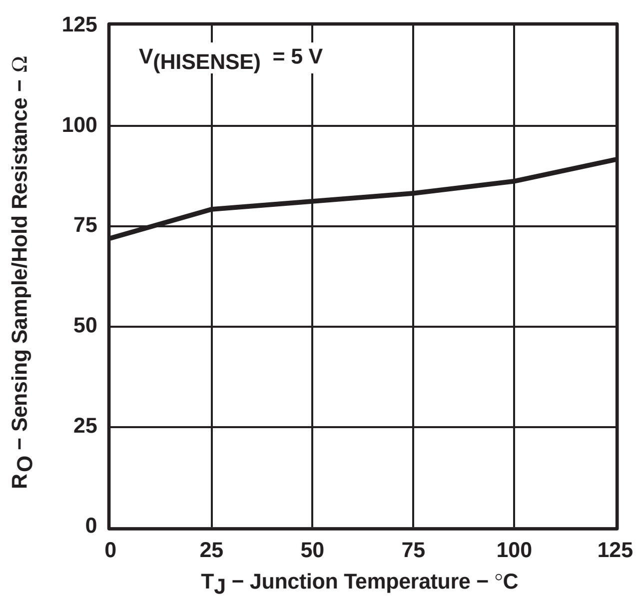


Figure 16

APPLICATION INFORMATION

The hysteretic-type controller method used in the TPS56100 controller gives very fast transient response for today’s high-speed DSP applications. Traditional PWM-type controllers use an oscillator to control the timing of the control signals used to adjust the output voltage. During a transient load event, the PWM-type controller must wait until the next oscillator cycle to begin the output voltage adjustment process. This delay causes output droop (or overshoot) and longer recovery times. Hysteretic-type controllers, such as the TPS56100, are self-oscillating and require no cycle-time to begin the recovery process. Hysteretic controllers have extremely high gain and are sensitive to noise. The TPS56100 has internal low-pass noise filters to eliminate much of this problem, however an external RC low-pass filter between the output and VSENSE input is recommended.

The TPS56100 controller includes all of the functions necessary for a dependable high-efficiency power converter. High-current synchronous MOSFET drivers are used for fast, low-loss switching allowing for efficiencies greater than 90%. An internal bootstrap circuit provides the high-side drive voltage necessary for the upper n-channel MOSFET. Overcurrent protection protects the power supply in case of load faults. Overvoltage protection protects the load in case of high-side switch failure. Programmable hysteresis allows users to tailor the output ripple and operating frequency to suit their needs. Slowstart provides a controlled rampup time for the output voltage eliminating output overshoot. Inhibit is provided for sequencing of the converter in multiple-voltage circuits. Power good provides an indication that the output voltage is within operating limits. The design of each of these functions is discussed in detail in the following. Refer to Figure 19 for location of components discussed in the following.

APPLICATION INFORMATION

frequency calculation

A detailed derivation of frequency calculation is shown in the application report, *Designing Fast Response Synchronous Buck Regulators Using the TPS5210*, TI Literature number SLVA044. When less accurate results are acceptable, the simplified equation shown below can be used:

$$f_S \cong \frac{\left(V_O \times \left[V_I - V_O\right] \times ESR\right)}{\left(V_I \times L \times \text{Hysteresis Window}\right)}$$

control section

Below are the equations needed to select the various components within the control section. Component reference numbers refer to the example application given at the end of this section. Details and the derivations of the equations used in this section are available in the application report *Designing Fast Response Synchronous Buck Regulators Using the TPS5210*, TI Literature number SLVA044.

output voltage selection

Of course the most important function of the power supply is to regulate the output voltage to a specific value. Values between 1.3 V and 2.6 V can be easily set by shorting the correct VP inputs to ground. Values above the maximum reference voltage (2.6 V) can be set by changing the reference voltage to any convenient voltage within its range and selecting values for R2 and R3 to give the correct output. Select R3:

R3 << than $V_{REF}/I_{BIAS(VSENSE)}$; a recommended value is 10 kΩ

Then, calculate R2 using:

$$V_O = V_{REF}\left(1 + \frac{R2}{R3}\right) \text{ or } R2 = \frac{R3 \times \left(V_O - V_{REF}\right)}{V_{REF}}$$

R2 and R3 can also be used to make small adjusts to the output voltage within the reference-voltage range. If there is no need to adjust the output voltage, R3 can be eliminated. R2, R3 (if used), and C7 are used as a noise filter; calculate using:

$$C7 = \frac{150 \text{ ns}}{\left(R2 \parallel R3\right)}$$

Recommended values for 3.3 V: V_{REF} = 1.65 V, R3 = 1.00 kΩ, R2 = 1.00 kΩ, and C7 = 100 pF.

slowstart timing

Slowstart reduces the start-up stresses on the power-stage components and reduces the input current surge. Slowstart timing is a function of the reference-voltage current (determined by R5) and is independent of the reference voltage. The first step in setting slowstart timing will be to determine R5:

R5 should be between 7 kΩ and 300 kΩ, a recommended value is 20 kΩ.

APPLICATION INFORMATION

slowstart timing (continued)

Set the slowstart timing using the formula:

$$C5 = \frac{t_{SS}}{\left(5 \times R_{VREFB}\right)} \cong \frac{t_{SS}}{(5 \times R5)}$$

Where

C5 = Slowstart capacitance in µF
t_{SS} = Slowstart timing in µs
R_{VREFB} = Resistance from VREFB to GND in ohms (≈ R5)

hysteresis voltage

A hysteretic controller regulates by self-oscillation, thus requiring a small ripple voltage on the output which the input comparator uses for sensing. Once selected, the TPS56100 hysteresis is proportional to the reference voltage; programming Vref to a new value automatically adjusts the hysteresis to be the same percentage of Vref. The actual output ripple voltage is the combination of the hysteresis voltage, overshoot caused by internal delays, and the output capacitor characteristics. Figure 19 shows the hysteresis window voltage (V_{HI} to V_{LO}) and the output voltage ripple (V_{MAX} to V_{MIN}). Since the output current from VREFB should be less than 500 µA, the total divider resistance (R4 + R5) should be greater than 7 kΩ. The hysteresis voltage should be no greater than 60 mV so R5 will dominate the divider.

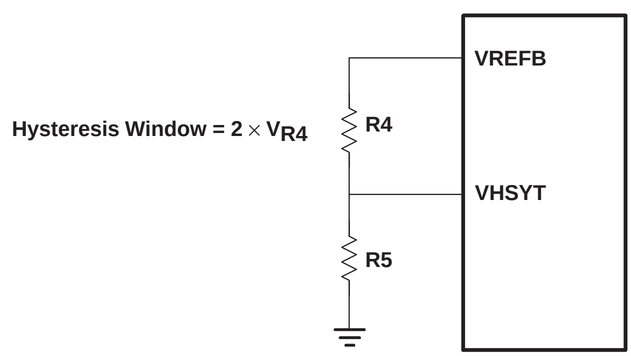


Figure 17. Hysteresis Divider Circuit

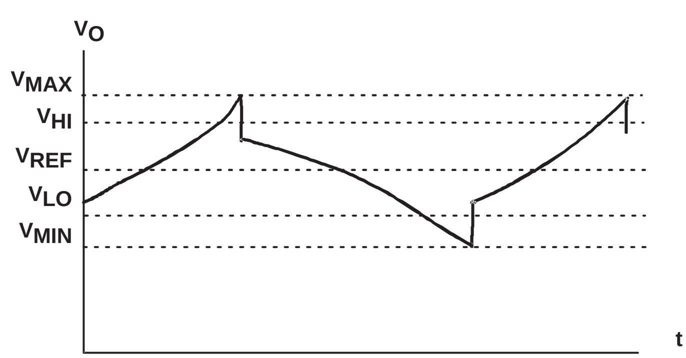


Figure 18. Output Ripple

APPLICATION INFORMATION

hysteresis voltage (continued)

The upper divider resistor, R4, is calculated using:

$$R4 = \frac{\text{Hysteresis Window}}{2 \times (\text{VREFB} - \text{Hysteresis Window})} \times R5 \cong \frac{V_{HYST}(\%)}{(2 \times 100)} \times R5$$

Where

Hysteresis Window = the desired peak-to-peak hysteresis voltage.
VREFB = selected reference voltage.
V_{HYST} (%) = [(Hysteresis Window)/VREFB] * 100 < $V_{O(Ripple)(P-P)}$ (%)

current limit

Current limit can be implemented using the on-resistance of the upper FETs as the sensing element. Select R7:

$$R7 \lll \frac{V_{OCP}}{I_{Bias(OCP)}} \leq \frac{0.1\ \text{V}}{(100 \times 100\ \text{nA})} \leq 10\ \text{k}\Omega \quad \text{(A recommended value is 1 k}\Omega\text{)}$$

The IOUT signal is used to drive the current limit divider. The voltage at IOUT at the output current trip point will be:

$$V_{IOUT(Trip)} = \frac{\left(2 \times R_{DS(ON)} \times TF\right)}{\text{NumFETs}} \times I_{O(Trip)}$$

Where

NumFETS = Number of upper FETS in Parallel.
TF = $R_{DS(ON)}$ temperature correction factor.
$I_{O(Trip)}$ = Desired output current trip level (A).

Calculate R6 using:

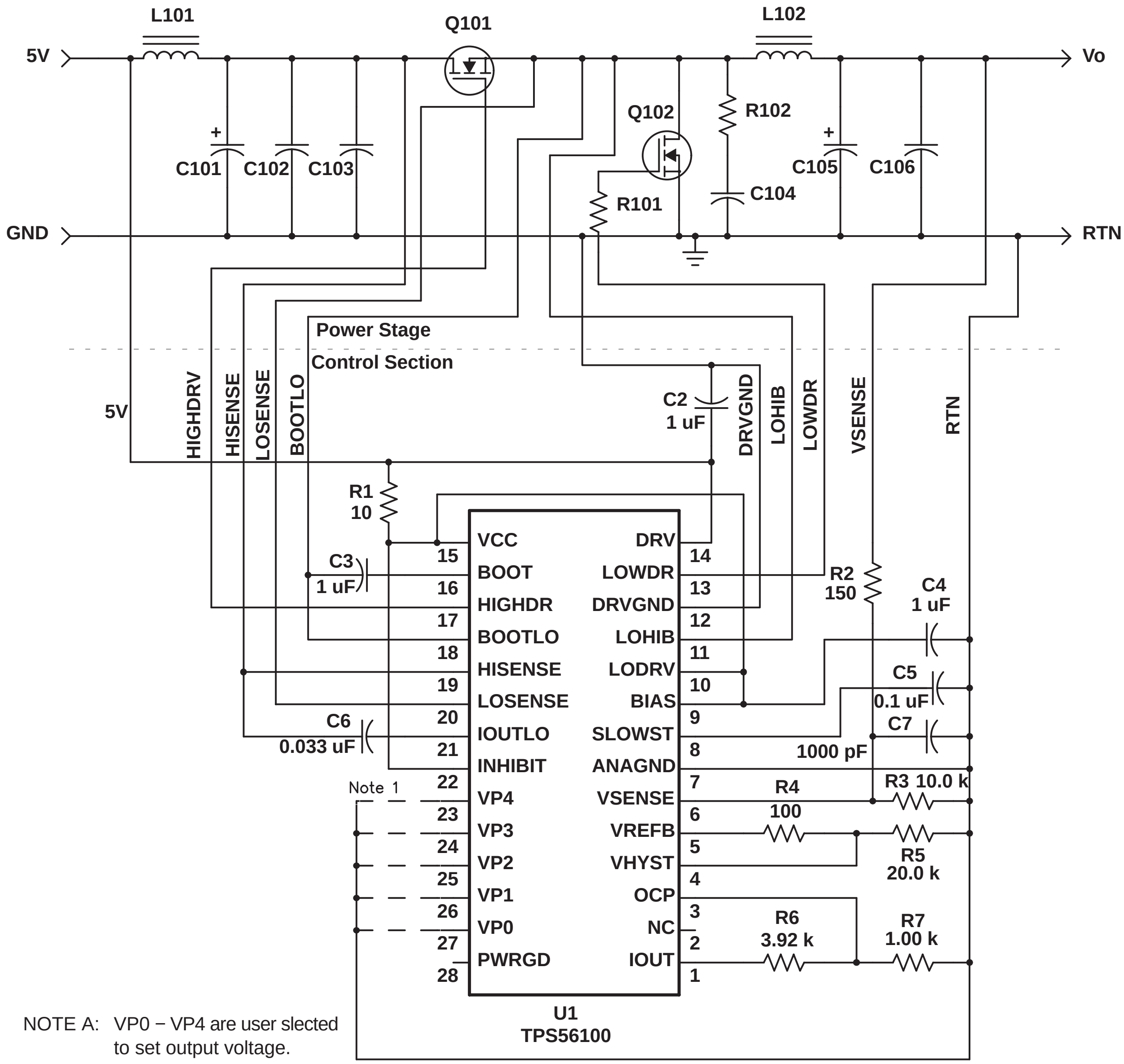
$$R6 = \left(\frac{V_{IOUT(Trip)}}{0.1\ \text{V}} - 1\right) \times R7$$

Note that since $R_{DS(ON)}$ of MOSFETs can vary from lot to lot and with temperature, tight current-limit control (less than 1.5 x I_O) using this method is not practical. If tight control is required, an external current-sense resistor in series with the drain of the upper FET can be used with HISENSE and LOSENSE connected across the resistor.

APPLICATION INFORMATION

application example

Below is a typical application schematic. The circuit can be divided into the power-stage section and the control-circuit section. The power stage must be tailored to the input/output requirements of the application. The control circuit is basically the same for all applications with some minor tweaking of specific values.



NOTE A: VP0 − VP4 are user slected to set output voltage. C1 is deleted.

Figure 19. Typical Application Schematic

APPLICATION INFORMATION

application example (continued)

Table 2. Power Stage Components

Ref Des	Function	4−A Out	8−A Out	12−A Out	20−A Out
C101	Input Bulk Capacitor	Sanyo, 10TPB220M, 220−µF, 10−V, 20%	Sanyo, 10SA220M, 2 x 220−µF, 10−V, 20%	Sanyo, 10SP470M, 2 x 470−µF, 10−V, 20%	Sanyo, 10SP470M, 3 x 470−µF, 10−V, 20%
C102	Input Mid−Freq Capacitor	muRata, GRM42−6Y5V105Z025A, 1.0−µF, 25−V, +80%−20%, Y5V	muRata, GRM42−6Y5V225Z016A, 2.2−µF, 16−V, +80%−20%, Y5V	muRata, GRM42−6Y5V225Z016A, 2.2−µF, 16−V, +80%−20%, Y5V	muRata, GRM42−6Y5V105Z025A, 3 x 1.0−µF, 25−V, +80%−20%, Y5V
C103	Input Hi−Freq Bypass Capacitor	muRata, GRM39X7R104K016A, 0.1−µF, 16−V, X7R	muRata, GRM39X7R104K016A, 0.1−µF, 16−V, X7R	muRata, GRM39X7R104K016A, 2 x 0.1−µF, 16−V, X7R	muRata, GRM39X7R104K016A, 3 x 0.1−µF, 16−V, X7R
C104	Snubber Capacitor	muRata, GRM39X7R102K050A, 1000−pF, 50−V, X7R	muRata, GRM39X7R102K050A, 1000−pF, 50−V, X7R	muRata, GRM39X7R102K050A, 2 x 1000 pF, 50−V, X7R	muRata, GRM39X7R102K050A, 3 x 1000−pF, 50−V, X7R
C105	Output Bulk Capacitor	Sanyo, 4TPC150, 2 x 150−µF, 4−V, 20%	Sanyo, 4SP820M, 820−µF, 4−V, 20%	Sanyo, 4SP820M, 2 x 820−µF, 4−V, 20%	Sanyo, 4SP820M, 3 x 820−µF, 4−V, 20%
C106	Output Hi−Freq Bypass Capaci-tor	muRata, GRM39X7R104K016A, 0.1−µF, 16−V, X7R	muRata, GRM39X7R104K016A, 0.1−µF, 16−V, X7R	muRata, GRM39X7R104K016A, 2 x 0.1−µF, 16−V, X7R	muRata, GRM39X7R104K016A, 3 x 0.1−µF, 16−V, X7R
L101	Input Filter Inductor	CoilCraft, DO1608C−332, 3.3−µH, 2.0−A	Coiltronics, UP2B−2R2, 2.2−µH, 7.2−A	Coiltronics, UP2B−2R2, 2.2−µH, 7.2−A	Coiltronics, UP3B−1R0, 1−µH, 12.5−A
L102	Output Filter Inductor	CoilCraft, DO3316P−332, 3.3−µH, 6.1−A	Coiltronics, UP3B−2R2, 2.2−µH, 9.2−A	Coiltronics, UP4B−1R5, 1.5−µH, 13.4−A	MicroMetals, T68−8/90 Core w/7T #16, 1.0−µH, 25−A
R101	Lo−Side Gate Resistor	3.3−Ω, 1/16−W, 5%	3.3−Ω, 1/16−W, 5%	2 x 3.3−Ω, 1/16−W, 5%	3 x 3.3−Ω, 1/16−W, 5%
R102	Snubber Resistor	2.7−Ω, 1/10−W, 5%	2.7−Ω, 1/10−W, 5%	2 x 2.7−Ω, 1/10−W, 5%	3 x 2.7−Ω, 1/10−W, 5%
Q101	Power Switch	IR, IRF7811, NMOS, 11−mΩ	IR, IRF7811, NMOS, 11−mΩ	IR, 2 x IRF7811, NMOS, 11−mΩ	IR, 2 x IRF7811, NMOS, 11−mΩ
Q102	Synchronous Switch	IR, IRF7811, NMOS, 11−mΩ	IR, IRF7811, NMOS, 11−mΩ	IR, 2 x IRF7811, NMOS, 11−mΩ	IR, 3 x IRF7811, NMOS, 11−mΩ
Nominal Frequency†		280 kHz	250 kHz	170 kHz	170 kHz
Hysteresis Window		15 mV	15 mV	15 mV	15 mV

† Nominal frequency measured with Vo set to 1.5 V.

The values listed above are recommendations based on actual test circuits. Many variations of the above are possible based upon the desires and/or requirements of the user. Performance of the circuit is equally, if not more, dependent upon the layout than on the specific components, as long as the device parameters are not exceeded. Fast-response, low-noise circuits require critical attention to the layout details. Even though the operating frequencies of typical power supplies are relatively low compared to today’s microprocessor circuits, the power levels and edge rates can cause severe problems both in the supply and the load. The power stage, having the highest current levels and greatest dv/dt rates, should be given the greatest attention.

APPLICATION INFORMATION

layout guidelines

Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens or even hundreds of amps, good power supply layout is much more difficult than most general PCB designs. The general design should proceed from the switching node to the output, then back to the driver section and, finally, place the low-level components. Below are several specific points to consider *before* layout of a TPS56100 design begins.

1. All sensitive analog components should be referenced to ANAGND. These include components connected to SLOWST, IOUT, OCP, VSENSE, VREFB, VHYST, BIAS, and LOHIB.
2. Analog ground and drive ground should be isolated as much as possible. Ideally, analog ground will connect to the ground side of the bulk storage capacitors on V_O, and drive ground will connect to the main ground plane close to the source of the low-side FET.
3. Connections from the drivers to the gate of the power FETs should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used.
4. The bypass capacitor for the DRV input should be placed close to the TPS56100 and be connected to DRVGND.
5. The bypass capacitor for V_{CC} should be placed close to the TPS56100 and be connected to AGND.
6. When configuring the high-side driver as a floating driver, the connection from BOOTLO to the power FETs should be as short and as wide as possible. The other pins that also connect to the power FETs, LOHIB and LOSENSE, should have a separate connection to the FETS since BOOTLO will have large peak currents flowing through it.
7. When configuring the high-side driver as a floating driver, the bootstrap capacitor (connected from BOOT to BOOTLO) should be placed close to the TPS56100.
8. When configuring the high-side driver as a ground-referenced driver, BOOTLO should be connected to DRVGND.
9. The bulk storage capacitors across V_I should be placed close to the power FETS. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and to the source of the low-side FET.
10. High-frequency bypass capacitors should be placed across the bulk storage capacitors on V_O.
11. HISENSE and LOSENSE should be connected very close to the drain and source, respectively, of the high-side FET. HISENSE and LOSENSE should be routed very close to each other to minimize differential-mode noise coupling to these traces. Ceramic decoupling capacitors should be placed close to where HISENSE connects to Vin, to reduce high-frequency noise coupling on HISENSE.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS56100PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS56100PWPG4	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS56100PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS56100PWPRG4	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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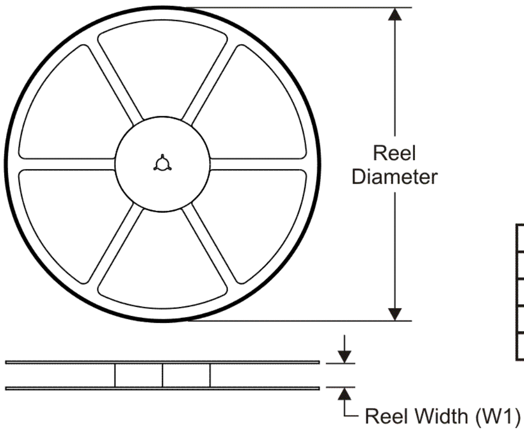
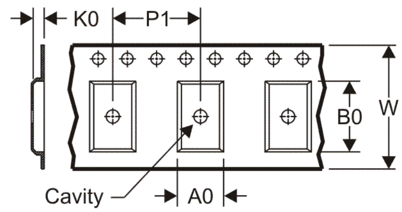
TAPE AND REEL INFORMATION

REEL DIMENSIONS

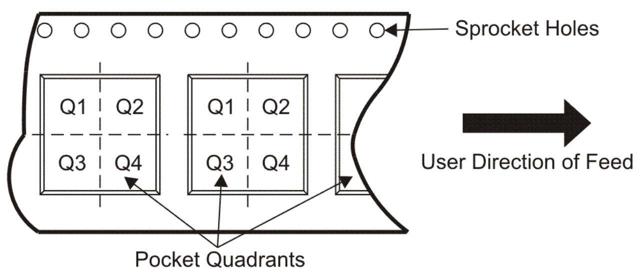


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

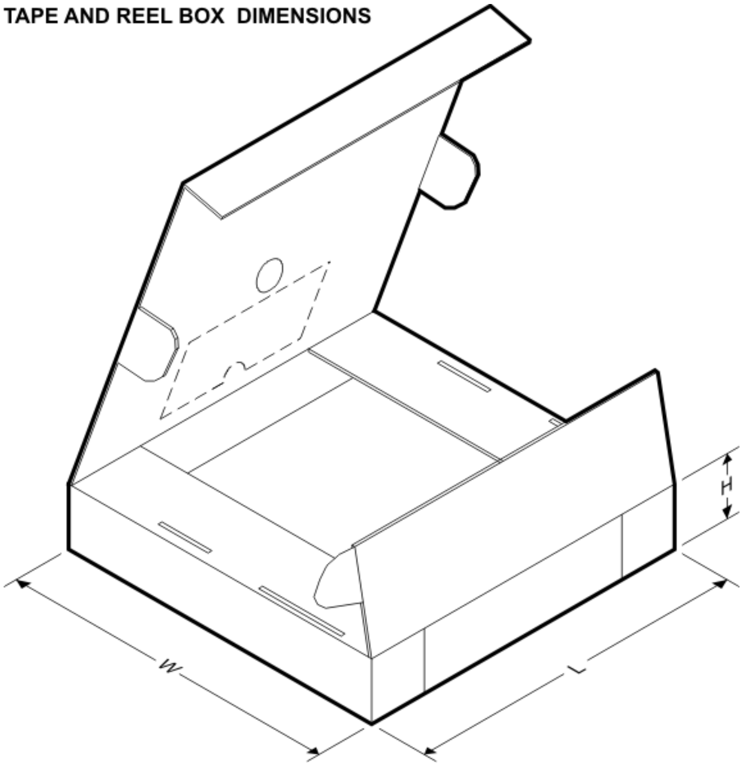
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS56100PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

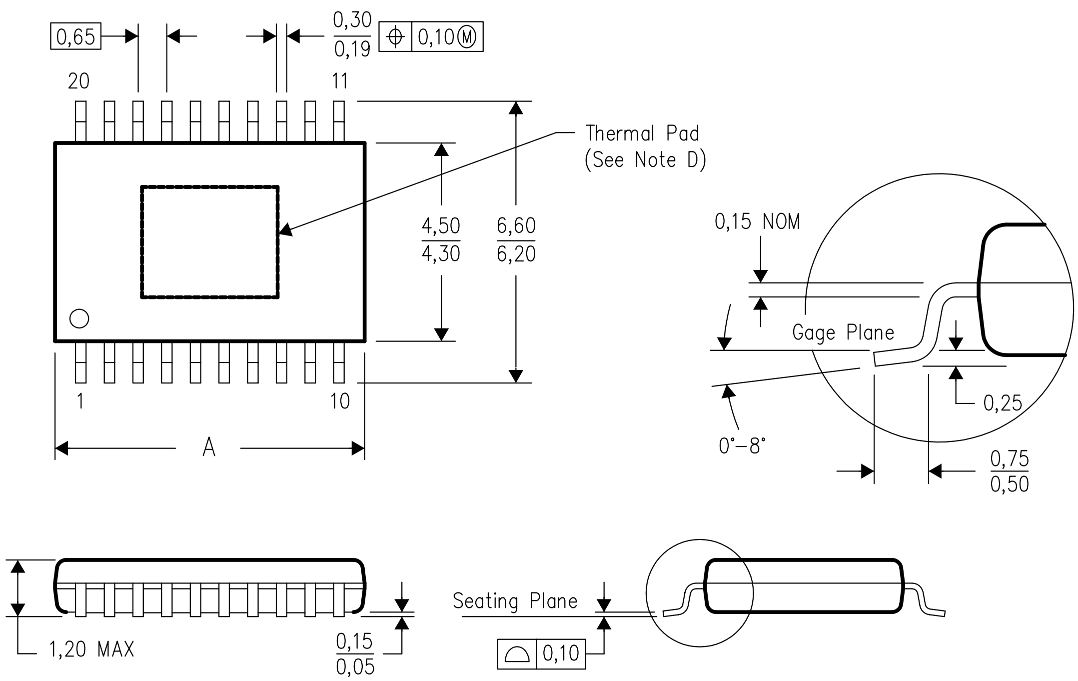


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS56100PWPR	HTSSOP	PWP	28	2000	346.0	346.0	33.0

PWP (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20 PIN SHOWN



PINS ** / DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. Falls within JEDEC MO-153

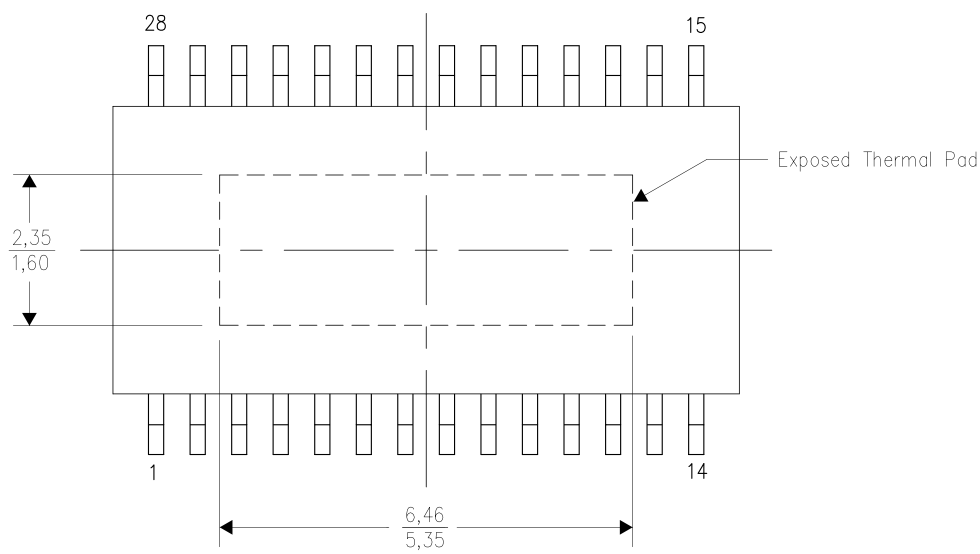
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

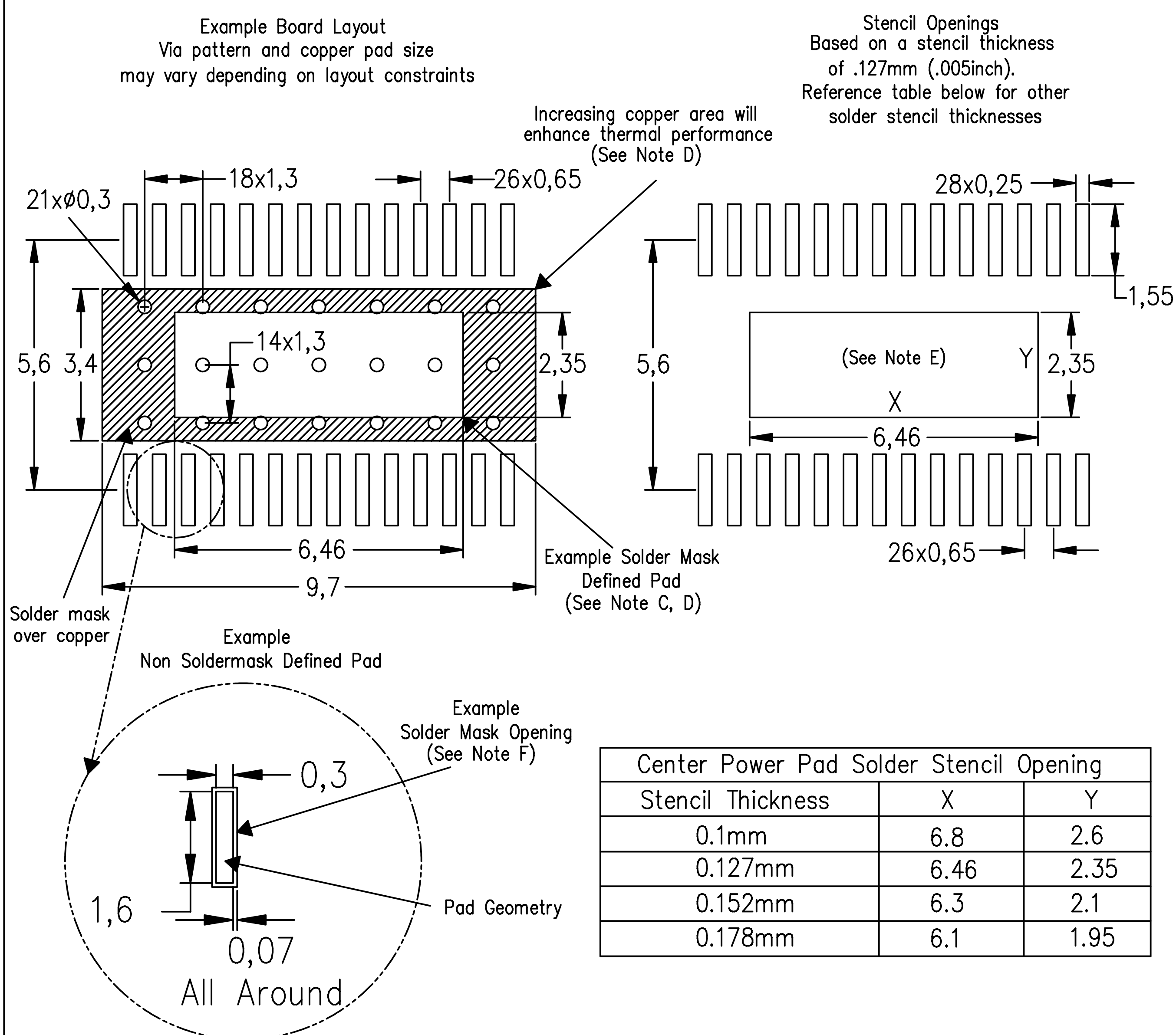


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R–PDSO–G28) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.8	2.6
0.127mm	6.46	2.35
0.152mm	6.3	2.1
0.178mm	6.1	1.95

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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